Pillsbury Ref: 81674/249727

WHAT IS CLAIMED IS:

1. A method, comprising:

receiving at least one packet;

issuing a receive interrupt with a delay, the delay being determined based on backlog information on a host, to inform the host about the received packets;

processing, upon receiving the receive interrupt, the received packets.

2. The method according to claim 1, wherein said issuing comprises:

determining the delay based on the backlog information gathered according to number of the processed packets that are returned from the host;

asserting the delay;

generating the receive interrupt, after the delay is asserted; and sending the receive interrupt to the host.

3. The method acording to claim 2, further comprising:

populating the at least one packet, after said receiving, into a packet buffer; and sending the received packets in the packet buffer to the host for said processing.

4. A method for an input and output controller, comprising:

receiving at least one packet;

populating the at least one packet into a packet buffer;

issuing a receive interrupt with a delay, determined based on backlog information on a host, to inform the host about the received packets; and

Pillsbury Ref: 81674/249727

sending the received packets to the host.

5. The method according to claim 4, wherein said issuing comprises:

gathering backlog information based on number of processed packets that are returned from the host;

determining the delay according to the backlog information;

asserting the delay;

generating the receive interrupt, after the delay is asserted; and

sending the receive interrupt to the host.

6. The method according to claim 5, wherein said determining the delay comprises:

determining a backlog zone using the backlog information; and

computing the delay based on a delay function for the backlog zone.

7. The method according to claim 6, wherein the delay function for the backlog zone

includes at least one of:

a constant function with a constant pre-determined according to the backlog zone;

a linear function defined within the backlog zone; or

a non-linear function defined within the backlog zone.

8. The method according to claim 7, further comprising:

allocating the packet buffer prior to said receiving; and

Pillsbury Ref: 81674/249727

populating the at least one packet into the packet buffer prior to said sending the received packets to the host.

9. A system, comprising:

an input and output controller for receiving packets and for notifying the received packets by sending a receive interrupt with an appropriate delay determined based on backlog information; and

a host for processing the received packets upon intercepting the receive interrupt and for returning processed packets to the input and output controller, from which the backlog information is determined.

10. The system according to claim 9, wherein said input and output controller comprises:

a packet receiver for intercepting the packets;

a packet buffer for storing the received packets; and

a backlog based interrupting mechanism for generating the receive interrupt, after the packets are populated in the packet buffer, based on the backlog information.

11. The system according to claim 10, wherein the backlog based interrupting mechanism comprises:

a delay determination mechanism for computing the appropriate delay based on the backlog information; and

Pillsbury Ref: 81674/249727

an interrupt generation mechanism for generating the receive interrupt with the appropriate delay and for sending the receive interrupt and the received packets to the host.

12. The system according to claim 10, wherein the host comprises:

an interrupt handler for intercepting and processing the receive interrupt; and
a protocol stack with at least one layer for handling the received packets at appropriate
layers.

13. The system according to claim 12, wherein said protocol stack comprises:

a packet processing mechanism for processing the received packets; and
a packet return mechanism for returning processed packets to the input and output
controller.

14. An input and output controller, comprising:

a packet receiver for intercepting at least one packet;

a packet buffer for storing the received packets; and

a backlog based interrupting mechanism for issuing a receive interrupt with an appropriate delay, computed based on backlog information, to a host.

15. The system according to claim 14, wherein the delay-based interrupting mechanism comprises:

a delay determination mechanism for computing the appropriate delay according to the the backlog information; and

Pillsbury Ref: 81674/249727

an interrupt generation mechanism for generating the receive interrupt with the appropriate delay and for sending the receive interrupt to the host.

16. The system according to claim 15, further comprising:

a buffer allocation mechanism for allocating the packet buffer; and

a packet population mechanism for populating the received packets into the packet

buffer.

17. A machine-accessible medium encoded with data, the data, when accessed,

causing:

receiving at least one packet;

issuing a receive interrupt with a delay, determined based on backlog information on a

host, to inform the host about the received packets;

processing, upon receiving the receving interrupt, the received packets; and

returning processed packets to an input and output controller.

18. The medium according to claim 17, wherein said issuing comprises:

determining the delay based on the backlog information gathered according to number

of the processed packets that are returned from the host;

asserting the delay;

generating the receive interrupt, after the delay is asserted; and

sending the receive interrupt to the host.

Pillsbury Ref: 81674/249727

19. The medium according to claim 18, the data, when accessed, further causing:

populating the at least one packet, after said receiving, into a packet buffer in the input and output controller;

intercepting the receive interrupt, prior to said processing; and sending the received packets to the host for said processing.

20. A machine-accessible medium encoded with data for an input and output controller, the data, when accessed, causing:

receiving at least one packet;

populating the at least one packet into a packet buffer;

issuing a receive interrupt with a delay, determined based on backlog information on a host, to inform the host about the received packets; and

sending the received packets to a host.

21. The medium according to claim 20, wherein said issuing comprises:

gathering backlog information based on number of processed packets that are returned from the host;

determining the delay according to the backlog information;

asserting the delay;

generating the receive interrupt, after the delay is asserted; and

sending the receive interrupt to the host.

Pillsbury Ref: 81674/249727

22. The medium according to claim 21, wherein said determining the delay comprises:

determining a backlog zone using the backlog information; and computing the delay based on a delay function for the backlog zone.

23. The medium according to claim 22, wherein the delay function for the backlog zone includes at least one of:

a constant function with a constant pre-determined according to the backlog zone;

a linear function defined within the backlog zone; or

a non-linear function defined within the backlog zone.

24. The medium according to claim 23, the data, when accessed, further causing: allocating the packet buffer prior to said receiving; and populating the at least one packet into the packet buffer prior to said sending the

received packets to the host.